Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.105”**

**.3 1 24**

**4**

**5**

**6**

**7**

**8**

**9**

**10**

**11 12 13 14**

**23**

**22**

**21**

**20**

**19**

**18**

**17**

**16**

**15**

**HI565A**

**MASK**

**REF**

**PAD FUNCTION:**

1. **Substrate Tie**
2. **VCC**
3. **REF OUT (+10V)**
4. **REF GND**
5. **REF IN**
6. **–VEE**
7. **BIPOLAR RIN**
8. **IDAC OUT**
9. **10V SPAN**
10. **20V SPAN**
11. **POWER GND**
12. **BIT 12 (LSB)**
13. **BIT 11**
14. **BIT 10**
15. **BIT 9**
16. **BIT 8**
17. **BIT 7**
18. **BIT 6**
19. **BIT 5**
20. **BIT 4**
21. **BIT 3**
22. **BIT 2**
23. **BIT 1 (MSB)**

**.179”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size = .004” X .004” min.**

**Backside Potential:**

**Mask Ref: HI565A**

**APPROVED BY: DK DIE SIZE .105” X .179” DATE: 8/25/21**

**MFG: HARRIS THICKNESS .019” P/N: HIO-0565A-2**

**DG 10.1.2**

#### Rev B, 7/1